ABSTRACT OF THE DISCLOSURE

A floating gate pixel is described which is formed by forming an N well in a P type silicon substrate. A P well is formed in the N well A gate is formed over a thin gate oxide, about 25 Angstroms thickness, such that the gate is directly over part of the P well and part of the N well. A P^+ contact in the P well allows connection to a reset voltage source, usually through a reset transistor, to reset the pixel. The pixel is reset by setting the potential between the P well and the substrate, which is usually held at ground potential. When the pixel is reset tunneling current through the thin gate oxide sets the voltage of the floating gate. During the charge integration cycle an input signal to the pixel, such as a light signal, changes the potential of the pixel. After the charge integration cycle the tunneling current through the gate oxide changes the potential of the floating gate by an amount related to the input signal to the pixel. The potential of the floating gate can then be read out to determine the input signal to the pixel. The pixel can also be embodied using a P well formed in an N type substrate, an N well formed in the P well, and an N^+ contact formed in the N well.